Amendments to the Specification

Please replace the paragraph beginning at page 6, line 16 with the following amended paragraph:

Referring to FIG. 2, the network processor 18 includes a processor 26 coupled to a first memory 30, a second memory 32, and a third memory 17. The third memory 17 has software instructions for managing the operation of the network processor 18. However, the instructions also can be stored in the first memory 30, the second memory 32, or a combination of the two memories. The processor 26 includes a queue manager ~~48~~ 27 containing software components configured to manage a cache of queue descriptors ("the cache") having a tag portion 44a and a data store portion 44b. The tag portion 44a of the cache 44 resides in the processor 26, whereas the data store portion 44b of the cache resides in the first memory 30. The tag portion 44a is managed by a content addressable memory (CAM) module 29 which can include hardware components configured to implement a cache entry replacement policy such as a least recently used (LRU) policy.